WHAT IS CLAIMED IS:

We claim:

1. A two-transistor PMOS memory cell, comprising:

a PMOS select transistor having a drain and a source formed as separate P+ diffusion regions in an N- well;

a PMOS floating gate transistor having a drain and a source formed as separate P+ diffusion regions in the N-well, wherein the P+ diffusion region that forms the floating gate transistor's drain is the same P+ diffusion region that forms the select gate transistor's source; and

an N implant underlying the P+ diffusion region that forms the floating gate transistor's drain.

2. The two-transistor PMOS memory cell of claim 1, wherein the lateral extent of the N implant is substantially the same as the lateral extent of the P+ diffusion region that forms the PMOS floating gate transistor's drain.

3. The two-transistor PMOS memory cell of claim 2, wherein the drain of the PMOS select transistor couples to a bit line of a memory array, and wherein a select gate of the PMOS select transistor couples to a word line of the memory array.

4. The two-transistor PMOS memory cell of claim 2, wherein a floating gate of the PMOS floating gate transistor is formed in a first polysilicon layer, and wherein a control gate of the PMOS floating gate transistor is formed in a second polysilicon layer.

5. The two-transistor PMOS memory cell of claim 2, wherein the memory cell includes a

single polysilicon layer containing a floating gate of the PMOS floating gate transistor, and wherein a control gate of the PMOS floating gate transistor is formed as a P+ diffusion region in the N- well.

6. The two-transistor PMOS memory cell of claim 2, wherein the memory cell is configured such that the floating gate transistor may be programmed using band-to-band tunneling.

7. The two-transistor PMOS memory cell of claim 2, wherein the memory cell is configured such that the floating gate transistor may be programmed using Fowler Nordheim tunneling.

8. The two-transistor PMOS memory cell of claim 2, wherein the P+ diffusion region that forms the floating gate transistor's drain has a thickness of approximately 0.1 to 0.25 microns.

9. The two-transistor PMOS memory cell of claim 2, wherein the thickness of the N implant underlying the P+ diffusion region that forms the floating gate transistor's drain is approximately 0.1 to 0.25 microns.

10. A process for manufacturing a two-transistor PMOS memory cell comprising:

forming an N- well in a P- substrate;

forming a tunnel oxide and a select gate channel oxide on a surface of the N- well;

forming a floating gate over the tunnel oxide and a select gate over the select gate channel oxide;

implanting an P-type dopant into the N- well through the floating gate and the select gate to form a first, a second, and a third P + diffusion region, the second P+ diffusion region located

between a first end of the floating gate and a first end of the select gate, the first P+ diffusion region located at an opposite end of the floating gate, and the third P+ diffusion region located at an opposite end of the select gate;

masking the first and third P+ diffusion regions; and

implanting an n-type dopant into the masked N-well region to form an N implant underlying the second P+ diffusion region.

11. The process of claim 10, wherein the process is a single polysilicon layer process, and wherein the act of forming the floating gate and the select gate comprises forming the gates in the single polysilicon layer.

12. The process of claim 10, wherein the process is a double polysilicon layer process, wherein the acto of forming the floating gate and the select gate comprises forming the gates in a first polysilicon layer, the method further comprising:

forming a control gate in a second polysilicon layer.

13. The method of claim 10, further comprising:

forming a bit line and a word line for programming the two-transistor PMOS memory cell.

14. The method of claim 10, further comprising:

manufacturing an array of the two-transistor PMOS memory cells.